REMARKS

Claims 1-5 and 7-12 are pending in this application, of which claims 8-12 are withdrawn from consideration. With the present Response, claims 1 and 7 are amended, and claim 6 is canceled. No new matter is added.

The drawings are objected to as failing to comply 37 C.F.R. § 1.84(p)(4), because reference character "25C" is used to denote the conductive wall inside interlayer insulation film 24. Attached with the present Response is a proposed drawing change to replace reference character "25C" in interlayer insulation film 24 with --24C--. The specification provides support for the proposed amendment, for example, on p. 3, lines 9-10. Accordingly, entry of the proposed amendment is hereby requested.

Claims 1-5 and 7 stand rejected under 35 U.S.C. § 103 as obvious over the prior art depicted in the present application, labeled "Admitted Prior Art (APA)," in view of *Cook et al.* (U.S. Patent No. 6,022,791) and *Chiang et al.* (U.S. Patent No. 5,817,572). Applicant responds as follows:

Base claim 1, as amended (i.e., to include feature previously recited in canceled claim 6), describes the interlayer insulation films as comprising a "first insulation film" and "second insulation film" that laterally support a "conductive wall" and a "conductive pattern," respectively. None of the APA interlayer insulation films 23, 24, and 25 include two insulation films as claimed. To properly address claim 1, one insulation film of an interlayer insulation film would have to support

a conductive wall (i.e., wall 23B, 24B, or 25B) laterally and another insulation film of the same interlayer insulation film would have to support a conductive pattern (i.e., 24A, 25A, or 26A, respectively) laterally.

The Office Action addresses these claimed features in the first full paragraph of p. 6 (Regarding claim 6, ...). The rejection relies on the APA interlayer insulation film 24 supporting a conductive wall and a teaching in *Chiang et al.* In particular, the Office Action provides a cite to the *Chiang et al.* Fig. 25, which discloses an insulation film (dielectric layer 350) supporting conductive barrier layer 360 and conductive layer 361 laterally. It is then concluded that the APA and *Chiang et al.* render unpatentable an interlayer insulation film comprising a first insulation film supporting a conductive wall and second insulation supporting a conductive pattern laterally as claimed. Applicant respectfully disagrees.

To justify the obviousness rejection, there must be provided a suggestion to modify the semiconductor device in the APA Fig. 2 so that an interlayer insulation film, for example, interlayer insulation film 24, would comprise *two* insulation films such that one insulation film would laterally support conductive pattern 24A and another insulation film would laterally support the conductive wall (labeled "24C" upon entry of the proposed drawing change). However, the Office Action does not identify any suggestion to make this modification. Applicant acknowledges that the Office Action states that *Chiang et al.* teaches an insulation film (i.e., *one* insulation film) that supports a conductive pattern laterally; however, this is not a suggestion which would motivate one to modify

the APA interlayer insulation films. Applicant therefore asserts that the Office Action does not provide a valid motivation to modify the APA semiconductor device so that each interlayer insulating film would include a first insulation film and a second insulation film that laterally support a conductive wall and a conductive pattern, respectively, as claimed.

In view of the above-described distinction between the semiconductor device described in claim 1 and that of the applied prior art, and further in view of the lack of a valid motivation to modify the semiconductor devices of the applied prior art to achieve the claimed invention, applicant respectfully submits that claim 1 is allowable over the applied prior art. Because claims 2-5 and 7 depend from claim 1, those claims are also allowable for at least the reason of their dependencies.

In addition to the remarks above, applicant adds the following regarding the applied prior art:

Cook et al. is silent with respect to the CMP process. Thus, there can be no mention in *Cook et al.* regarding the use of an interlayer insulation film for laterally supporting a conductive via wall or a conductive pattern for use during the CMP process. Also, there is no teaching in *Cook* to use plural films in an interlayer insulation film for supporting the conductive wall and the conductive pattern separately.

The portions of the APA cited as support for the rejection are also silent with respect to the use of first and second insulation films within an interlayer insulation film for laterally supporting

the conductive wall and the conductive pattern separately.

Chiang et al. merely shows the use of two films in an interlayer insulation film. The reference is silent with respect to using a first film to support a conductive wall laterally and a second film to support a conductive pattern laterally.

Therefore, there can be no motivation for a person skilled in the art to combine the foregoing references to derive the subject matter of the present invention as set forth in amended claim 1, particularly without knowledge of the problem of the CMP process explained in the present invention with reference to Figs. 3A, 3B, 4, and 5. It is further noted that the problem described in *Cook et al.* is related to the dicing process using a rotating dicing blade and not the CMP process explained with reference to Fig. 4. Therefore, the knowledge of *Cook et al.* with regard to the problem of dicing does not provide a motivation for a person skilled in the art to modify the teaching of *Cook et al.* to derive the subject matter of the present invention.

In view of the amendments and remarks above, applicant now submits that the entire application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is felt that this application is not now in condition for allowance, the Examiner is invited to contact applicant's undersigned attorney at the telephone number indicated below to arrange for disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version of Amendments with Markings to Show Changes Made**."

In the event that this paper is not timely filed, applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully Submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version of amendments with markings to show changes made
Request for Approval of Drawing Changes

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VERSION OF AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Serial No.: 09/528,296

Cancel claim 6.

Amend claims 1 and 7 as follows:

1. (Three Times Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface

of said substrate when viewed in a direction perpendicular to said principal surface of said substrate, and wherein said interlayer insulation films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally.

7 (Amended) A semiconductor device as claimed in claim [6] 1, further comprising an etching stopper layer interposed between said first insulation film and said second insulation film.